



# DS1225Y

## 64k Nonvolatile SRAM

[www.maxim-ic.com](http://www.maxim-ic.com)

### FEATURES

- 10 years minimum data retention in the absence of external power
- Data is automatically protected during power loss
- Directly replaces 2k x 8 volatile static RAM or EEPROM
- Unlimited write cycles
- Low-power CMOS
- JEDEC standard 28-pin DIP package
- Read and write access times as fast as 150 ns
- Full  $\pm 10\%$  operating range
- Optional industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$ , designated IND

### PIN ASSIGNMENT

NC	1	28	VCC
A12	2	27	$\overline{\text{WE}}$
A7	3	26	NC
A6	4	25	A8
A5	5	24	A9
A4	6	23	A11
A3	7	22	$\overline{\text{OE}}$
A2	8	21	A10
A1	9	20	$\overline{\text{CE}}$
A0	10	19	DQ7
DQ0	11	18	DQ6
DQ1	12	17	DQ5
DQ2	13	16	DQ4
GND	14	15	DQ3

24-Pin ENCAPSULATED PACKAGE  
720-mil EXTENDED

### PIN DESCRIPTION

A0-A12	- Address Inputs
DQ0-DQ7	- Data In/Data Out
$\overline{\text{CE}}$	- Chip Enable
$\overline{\text{WE}}$	- Write Enable
$\overline{\text{OE}}$	- Output Enable
V <sub>CC</sub>	- Power (+5V)
GND	- Ground

### DESCRIPTION

The DS1225Y 64k Nonvolatile SRAM is a 65,536-bit, fully static, nonvolatile RAM organized as 8192 words by 8 bits. Each NV SRAM has a self-contained lithium energy source and control circuitry which constantly monitors V<sub>CC</sub> for an out-of-tolerance condition. When such a condition occurs, the lithium energy source is automatically switched on and write protection is unconditionally enabled to prevent data corruption. The NV SRAM can be used in place of existing 8k x 8 SRAMs directly conforming to the popular byte-wide 28-pin DIP standard. The DS1225Y also matches the pinout of the 2764 EPROM or the 2864 EEPROM, allowing direct substitution while enhancing performance. There is no limit on the number of write cycles that can be executed and no additional support circuitry is required for micro-processor interfacing.

## READ MODE

The DS1225Y executes a read cycle whenever  $\overline{WE}$  (Write Enable) is inactive (high) and  $\overline{CE}$  (Chip Enable) and  $\overline{OE}$  (Output Enable) are active (low). The unique address specified by the 13 address inputs ( $A_0$ - $A_{12}$ ) defines which of the 8192 bytes of data is to be accessed. Valid data will be available to the eight data output drivers within  $t_{ACC}$  (Access Time) after the last address input signal is stable, providing that  $\overline{CE}$  and  $\overline{OE}$  access times are also satisfied. If  $\overline{CE}$  and  $\overline{OE}$  access times are not satisfied, then data access must be measured from the later-occurring signal and the limiting parameter is either  $t_{CO}$  for  $\overline{CE}$  or  $t_{OE}$  for  $\overline{OE}$  rather than address access.

## WRITE MODE

The DS1225Y executes a write cycle whenever the  $\overline{WE}$  and  $\overline{CE}$  signals are active (low) after address inputs are stable. The later-occurring falling edge of  $\overline{CE}$  or  $\overline{WE}$  will determine the start of the write cycle. The write cycle is terminated by the earlier rising edge of  $\overline{CE}$  or  $\overline{WE}$ . All address inputs must be kept valid throughout the write cycle.  $\overline{WE}$  must return to the high state for a minimum recovery time ( $t_{WR}$ ) before another cycle can be initiated. The  $\overline{OE}$  control signal should be kept inactive (high) during write cycles to avoid bus contention. However, if the output drivers are enabled ( $\overline{CE}$  and  $\overline{OE}$  active) then  $\overline{WE}$  will disable the outputs in  $t_{ODW}$  from its falling edge.

## DATA RETENTION MODE

The DS1225Y provides full functional capability for  $V_{CC}$  greater than 4.5 volts and write protects at 4.25 nominal. Data is maintained in the absence of  $V_{CC}$  without any additional support circuitry. The DS1225Y constantly monitors  $V_{CC}$ . Should the supply voltage decay, the NV SRAM automatically write protects itself, all inputs become “don’t care,” and all outputs become high impedance. As  $V_{CC}$  falls below approximately 3.0 volts, a power switching circuit connects the lithium energy source to RAM to retain data. During power-up, when  $V_{CC}$  rises above approximately 3.0 volts, the power switching circuit connects external  $V_{CC}$  to RAM and disconnects the lithium energy source. Normal RAM operation can resume after  $V_{CC}$  exceeds 4.5 volts.

**ABSOLUTE MAXIMUM RATINGS\***

Voltage on Any Pin Relative to Ground	-0.3V to +7.0V
Operating Temperature	0°C to 70°C; -40°C to +85°C for IND parts
Storage Temperature	-40°C to +70°C; -40°C to +85°C for IND parts
Soldering Temperature	260°C for 10 seconds

\* This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect reliability.

**RECOMMENDED DC OPERATING CONDITIONS** ( $T_A$  : See Note 10)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Power Supply Voltage	$V_{CC}$	4.5	5.0	5.5	V	
Input Logic 1	$V_{IH}$	2.2		$V_{CC}$	V	
Input Logic 0	$V_{IL}$	0.0		+0.8	V	

**DC ELECTRICAL CHARACTERISTICS** ( $T_A$  : See Note 10;  $V_{CC} = 5V \pm 10\%$ )

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Leakage Current	$I_{IL}$	-1.0		+1.0	$\mu A$	
I/O Leakage Current $\overline{CE} \geq V_{IH} \leq V_{CC}$	$I_{IO}$	-1.0		+1.0	$\mu A$	
Output Current @ 2.4V	$I_{OH}$	-1.0			mA	
Output Current @ 0.4V	$I_{OL}$	2.0			mA	
Standby Current $\overline{CE} = 2.2V$	$I_{CCS1}$		5	10	mA	
Standby Current $\overline{CE} = V_{CC} - 0.5V$	$I_{CCS2}$		3	5	mA	
Operating Current $t_{CYC} = 200ns$ (Commercial)	$I_{CCO1}$			75	mA	
Operating Current $t_{CYC} = 200ns$ (Industrial)	$I_{CCO1}$			85	mA	
Write Protection Voltage	$V_{TP}$		4.25		V	10

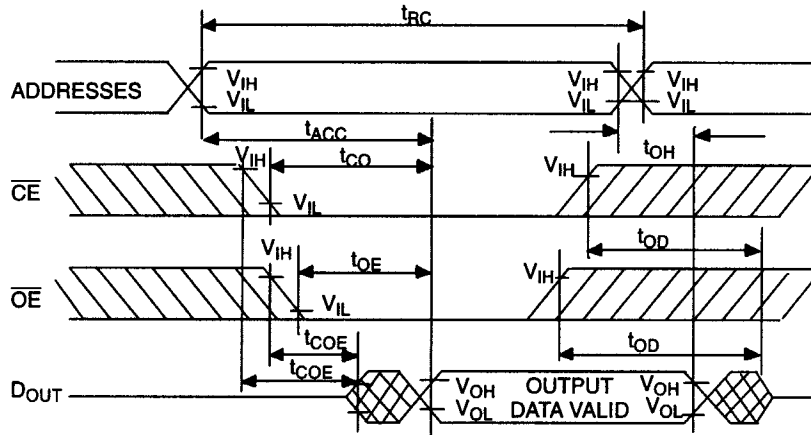
**AC ELECTRICAL CHARACTERISTICS** ( $t_A$ : See Note 10;  $V_{CC} = 5.0V \pm 10\%$ )

PARAMETER	SYMBOL	DS1225Y-150		DS1225Y-170		DS1225Y-200		UNITS	NOTES
		MIN	MAX	MIN	MAX	MIN	MAX		
Read Cycle Time	$t_{RC}$	150		170		200		ns	
Access Time	$t_{ACC}$		150		170		200	ns	
$\overline{OE}$ to Output Valid	$t_{OE}$		70		80		100	ns	
$\overline{CE}$ to Output Valid	$t_{CO}$		150		170		200	ns	
$\overline{OE}$ or $\overline{CE}$ to Output Active	$t_{COE}$	5		5		5		ns	5
Output High Z from Deselection	$t_{OD}$		35		35		35	ns	5
Output Hold from AddressChange	$t_{OH}$	5		5		5		ns	
Write Cycle Time	$t_{WC}$	150		170		200		ns	
Write Pulse Width	$t_{WP}$	100		120		150		ns	3
Address Setup Time	$t_{AW}$	0		0		0		ns	
Write Recovery Time	$t_{WR1}$	0		0		0		ns	12
	$t_{WR2}$	10		10		10		ns	13
Output High Z from $\overline{WE}$	$t_{ODW}$		35		35		35	ns	5
Output Active from $\overline{WE}$	$t_{OEW}$	5		5		5		ns	5
Data Setup Time	$t_{DS}$	60		70		80		ns	4
Data Hold Time	$t_{DH1}$	0		0		0		ns	12
	$t_{DH2}$	10		10		10		ns	13

**CAPACITANCE** $(T_A = 25^\circ C)$ 

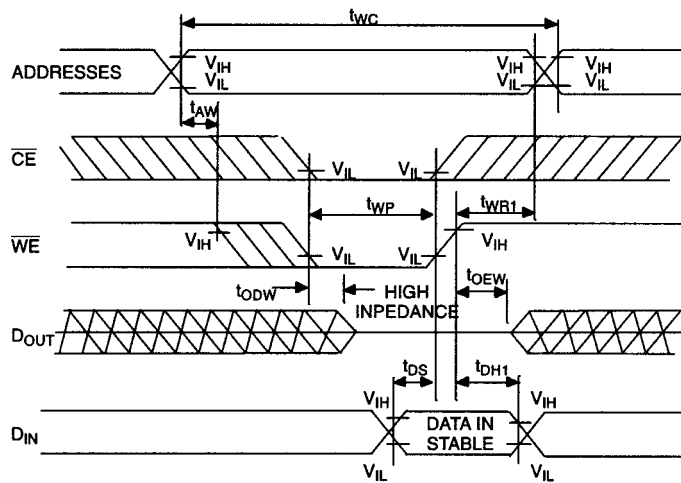
PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	NOTES
Input Capacitance	$C_{IN}$			10	pF	
Input/Output Capacitance	$C_{I/O}$			10	pF	

## READ CYCLE



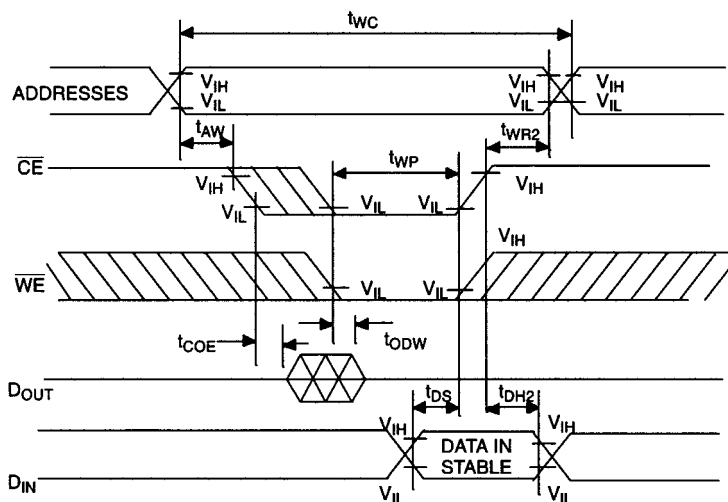
SEE NOTE 1

## WRITE CYCLE 1



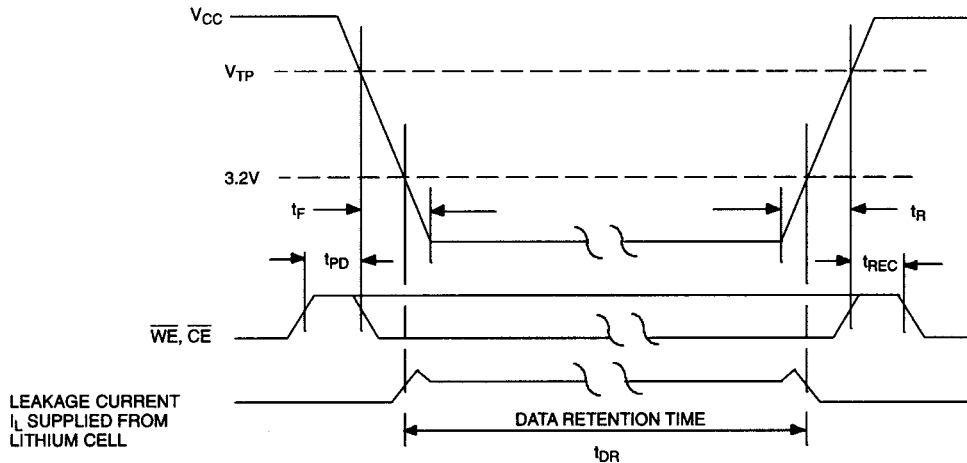
SEE NOTE 2, 3, 4, 6, 7, 8 AND 12

## WRITE CYCLE 2



SEE NOTE 2, 3, 4, 6, 7, 8 AND 13

## POWER-DOWN/POWER-UP CONDITION



SEE NOTE 11

## POWER-DOWN/POWER-UP TIMING

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
$\overline{CE}$ at $V_{IH}$ before Power-Down	$t_{PD}$	0		$\mu\text{s}$	11
$V_{CC}$ Slew from $V_{TP}$ to 0V	$t_F$	100		$\mu\text{s}$	
$V_{CC}$ Slew from 0V to $V_{TP}$	$t_R$	0		$\mu\text{s}$	
$\overline{CE}$ at $V_{IH}$ after Power-Up	$t_{REC}$		2	ms	

 $(T_A = 25^\circ\text{C})$ 

PARAMETER	SYMBOL	MIN	MAX	UNITS	NOTES
Expected Data Retention Time	$t_{DR}$	10		years	9

### WARNING:

Under no circumstance are negative undershoots, of any amplitude, allowed when device is in battery backup mode.

### NOTES:

- $\overline{WE}$  is high for a read cycle.
- $\overline{OE} = V_{IH}$  or  $V_{IL}$ . If  $\overline{OE} = V_{IH}$  during a write cycle, the output buffers remain in a high impedance state.
- $t_{WP}$  is specified as the logical AND of  $\overline{CE}$  and  $\overline{WE}$ .  $t_{WP}$  is measured from the latter of  $\overline{CE}$  or  $\overline{WE}$  going low to the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- $t_{DS}$  is measured from the earlier of  $\overline{CE}$  or  $\overline{WE}$  going high.
- These parameters are sampled with a 5 pF load and are not 100% tested.
- If the  $\overline{CE}$  low transition occurs simultaneously with or later than the  $\overline{WE}$  low transition in Write Cycle 1, the output buffers remain in a high-impedance state during this period.
- If the  $\overline{CE}$  high transition occurs prior to or simultaneously with the  $\overline{WE}$  high transition, the output buffers remain in a high-impedance state during this period.

8. If  $\overline{WE}$  is low or the  $\overline{WE}$  low transition occurs prior to or simultaneously with the  $\overline{CE}$  low transition, the output buffers remain in a high-impedance state during this period.
9. Each DS1225Y is marked with a 4-digit date code AABB. AA designates the year of manufacture. BB designates the week of manufacture. The expected  $t_{DR}$  is defined as starting at the date of manufacture.
10. All AC and DC electrical characteristics are valid over the full operating temperature range. For commercial products, this range is 0°C to 70°C. For industrial products (IND), this range is -40°C to +85°C.
11. In a power down condition the voltage on any pin may not exceed the voltage on  $V_{CC}$ .
12.  $t_{WR1}$ ,  $t_{DH1}$  are measured from  $\overline{WE}$  going high.
13.  $t_{WR2}$ ,  $t_{DH2}$  are measured from  $\overline{CE}$  going high.
14. DS1225Y modules are recognized by Underwriters Laboratory (U.L.®) under file E99151 (R).

### DC TEST CONDITIONS

Outputs open.

All voltages are referenced to ground.

### AC TEST CONDITIONS

Output Load: 100pF + 1TTL Gate

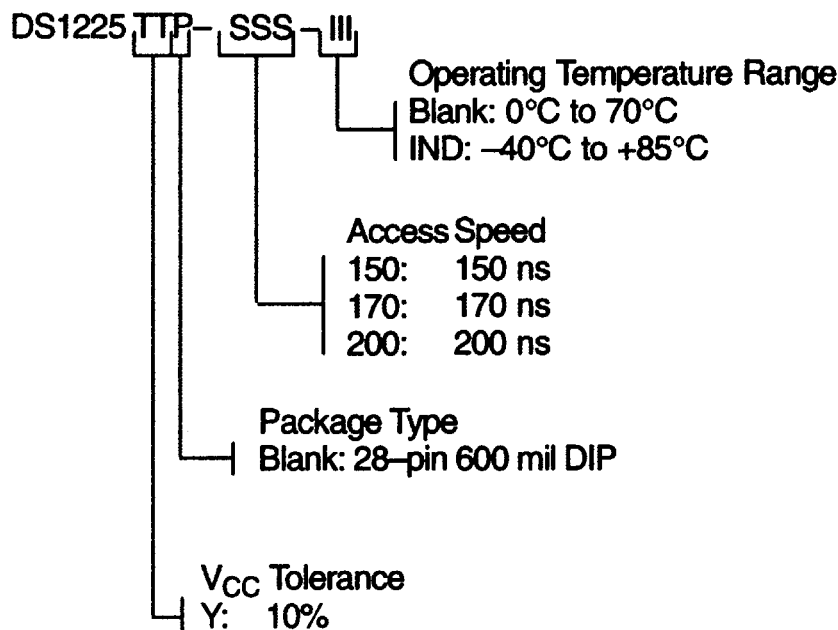
Input Pulse Levels: 0-3.0V

Timing Measurement Reference Levels

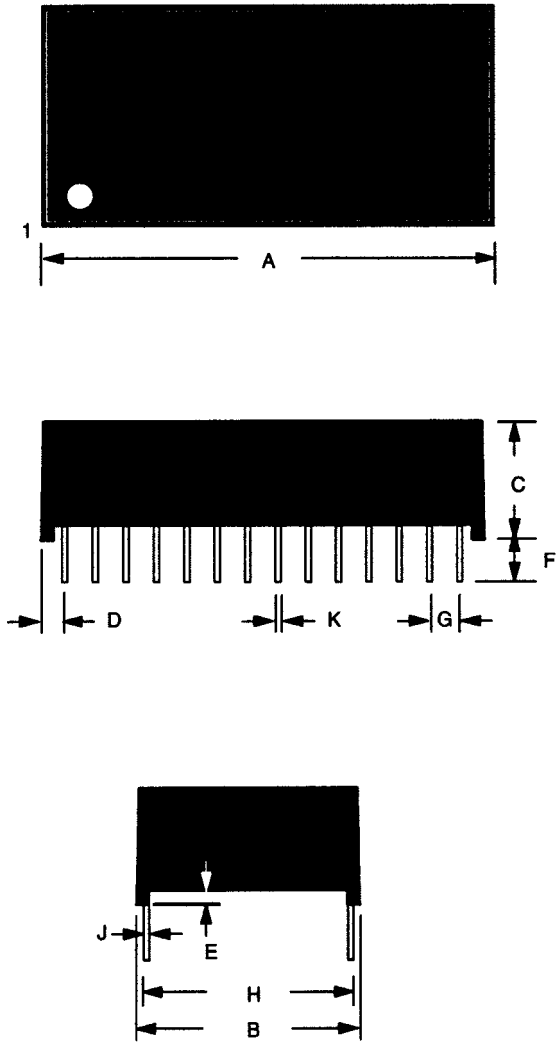
Input: 1.5V Output: 1.5V

Input Pulse Rise and Fall Times: 5ns

### ORDERING INFORMATION



# DS1225Y NONVOLATILE SRAM, 28-PIN, 720-MIL EXTENDED MODULE



PKG DIM	28-PIN	
	MIN	MAX
A IN.	1.520	1.540
MM	38.61	39.12
B IN.	0.695	0.720
MM	17.65	18.29
C IN.	0.395	0.415
MM	10.03	10.54
D IN.	0.100	0.130
MM	2.54	3.30
E IN.	0.017	0.030
MM	0.43	0.76
F IN.	0.120	0.160
MM	3.05	4.06
G IN.	0.090	0.110
MM	2.29	2.79
H IN.	0.590	0.630
MM	14.99	16.00
J IN.	0.008	0.012
MM	0.20	0.30
K IN.	0.015	0.021
MM	0.38	0.53